MERI College of Engineering & Technology
(MERI-CET)

Session: 2019-2020 **Course: CSE**

Lesson plan

Name of the faculty : Er. Gaurav Kumar

Discipline : CSE/ECE

Semester : 6th Semester

Subject : Digital System Design

Lesson Plan Duration : 15 weeks (From 4th Jan, 2020 to 20th April 2020)

Work Load (Lecture/ Practical) per week (in hours): Lecture-02, Practical-01

Week	Theory		Practical	
	Lecture day	Topic(Including assignment/test)	Practical Day	Topic
1st	1st	Introduction to Computer aided design tools for digital systems	1st	Design all gates using VHDL
	2nd	Introduction to Computer aided design tools for digital systems		
2nd	1st	Hardware description languages	2nd	Design all gates using VHDL
	2nd	Introduction to VHDL		
3rd	1st	Data objects, classes and data types	3rd	WAP in VHDL of Half Adder
	2nd	Operators.		
4th	1st	Types of delays Entity and Architecture declaration.	4th	WAP in VHDL of Full Adder
	2nd	Introduction to behavioral, dataflow and structural models.		
5th	1st	Vhdl Statements: Assignment statements, sequential statements	5th	WAP in VHDL of Full Adder
	2nd	Process, conditional statements,		
6th	1st	Case statement Array and loops, resolution functions	6th	WAP in VHDL of Multiplexer.
	2nd	Packages and Libraries, concurrent statements.		
7th	1st	Subprograms: Application of Functions and Procedures, Structural Modeling	7th	WAP in VHDL of DE Multiplexer
	2nd	Component declaration, structural layout and generics		
8th	1st	Combinational Circuit Design	8th	WAP in VHDL of Encoder.
	2nd	VHDL Models and Simulation of Multiplexers.		
9th	1st	VHDL Models and Simulation of DE multiplexers	9th	WAP in VHDL of Decoder.

	2nd	VHDL Models and Simulation of encoders		
10th	1st	VHDL Models and Simulation of decoders.	10th	
	2nd	Code converters		WAP in VHDL of Comparator.
11th	1st	Implementation of Boolean functions etc.	11th	WAP in VHDL of Comparator.
	2nd	Comparators, Sequential Circuits Design		
12th	1st	VHDL Models and Simulation of Sequential Circuits.	12th	
	2nd	VHDL Models and Simulation of Shift Registers, Counters		WAP in VHDL of Code converter.
13th	1st	Design Of Microcomputer: Basic components of a computer, ,	13th	
	2nd	specifications architecture of a simple microcomputer system		Internal Practical
14th	1st	Implementation of a simple microcomputer system using VHDL.	14th	
	2nd	Programmable logic devices: ROM, PLAs, PALs		Internal Practical
15th	1st	GAL, PEEL, CPLDs and FPGA .	15th	External Practical.
	2nd	Design implementation using CPLDs and FPGAs		

REFERENCE BOOKS:

1. IEEE Standard VHDL Language Reference Manual (1993).
2. Digital Design and Modelling with VHDL and Synthesis : KC Chang; IEEE Computer Society Press.
3. "A VHDL Primmer" : Bhasker; Prentice Hall 1995.
4. "Digital System Design using VHDL" : Charles. H.Roth ; PWS (1998).
5. "VHDL-Analysis & Modelling of Digital Systems" : Navabi Z; McGraw Hill.
6. VHDL-IV Edition :Perry; TMH (2002)
7. "Introduction to Digital Systems" : Ercegovac. Lang & Moreno; John Wiley (1999).
8. Fundamentals of Digital Logic with VHDL Design : Brown and Vranesic; TMH (2000)
9. Modern Digital Electronics- III Edition: R.P Jain; TMH (2003).